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NO. 588 P. 1

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**To:**

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**FROM:** Robert E. Scheid (Reg. No. 42,126)**DATE:** November 15, 2004

Number of pages with cover page: 6

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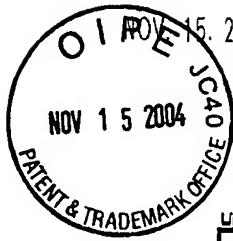
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**Contents of this Transmission:**

Inventor: David LEWIS et al.	Atty Docket No. 306812002500:
Application No.: 10/057,232	Filing Date: January 25, 2002
Group Art Unit: 2825	Examiner: L. H. Malsawma
Title: SYSTEM AND METHOD FOR ASYMMETRIC ROUTING LINES	
Documents Filed:	
Transmittal (1 page)	
Statement of the Substance of the Interview (2 pages)	
Examiner's Amendment to the Claims (2 pages)	
Facsimile Return Receipt Cover	
Sender's Initials:	RES4/jxh3
Date	November 15, 2004

sf-1816652

PAGE 1/6 \*RCVD AT 11/15/2004 5:54:11 PM [Eastern Standard Time]\* SVR:USPTO-EFXRF-2/0 \* DNIS:7464000 \* CSID:415 2687522 \* DURATION (mm:ss):01:58



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NO. 588 P. 2

PTO/SB/21 (04-04)

Approved for use through 07/31/2008. OMB 0651-0031  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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## TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

		Application Number	10/057,232
		Filing Date	January 25, 2002
		First Named Inventor	David LEWIS
		Art Unit	2825
		Examiner Name	L. H. Malsawma
Total Number of Pages in This Submission	5	Attorney Docket Number	308812002500

### ENCLOSURES (Check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s)	<input type="checkbox"/> After Allowance communication to Technology Center (TC) <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): Statement of the Substance of the Interview (2 pages) Examiner's Amendment Revisions (2 pages) Facsimile Return Receipt Cover
		Remarks

### SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	MORRISON & FOERSTER LLP (Customer No. 20872) Robert E. Scheid - 42,126
Signature	
Date	November 15, 2004

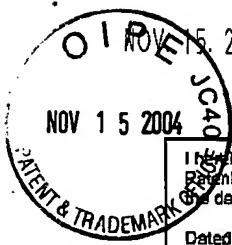
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Signature: (Janet Hollrah)

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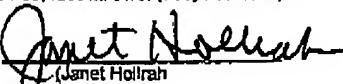


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Dated: November 15, 2004 Signature:   
(Janet Holrah)

Docket No.: 306812002500  
(PATENT)

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
David LEWIS et al.

Application No.: 10/057,232

Art Unit: 2825

Filed: January 25, 2002

Examiner: L. H. Malsawma

For: **SYSTEM AND METHOD FOR ASYMMETRIC  
ROUTING LINES**

### STATEMENT OF THE SUBSTANCE OF THE INTERVIEW

MS Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

This is to summarize a telephonic interviews between the undersigned, Examiner Lex Malsawma and Leigh Garbowski on October 6 and 8, 2004, concerning claims 1, 9, 15, 16, 17 and 20. Claim 1 was discussed in detail and a tentative agreement was reached to amend claims 1, 9, 15, 16, 17 and 20. Attached to this Statement of the Substance of the Interview are the aforesaid claims showing the changes made in the Examiner's Amendment, which was included in the Notice of Allowance papers dated October 19, 2004. This Statement is filed within the time frame of one month from the date of the Notice of Allowance and thereby is timely filed.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection

sf-1813207

Application No.: 10/057,232

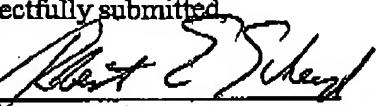
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Docket No.: 306812002500

with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 306812002500. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: November 15, 2004

Respectfully submitted,

By   
Robert E. Scheid

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sf-1813207



Examiner's Amendment Revisions  
Notice of Allowance of October 19, 2004  
U.S. Patent Application No. 10/057,232

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**Claim 1 (Currently Amended):** Within a programmable logic device, a routing architecture to interconnect a plurality of function blocks, comprising:

a plurality of wires oriented in a first direction, wherein the wires oriented in the first direction have a physical length that is substantially the same as an electrically optimum physical length or the an adjustment of the electrically optimum physical length to account for non-electrical considerations.

**Claim 9 (Currently Amended):** Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a wire having a logical length that is a function of an orientation of the wire and having a physical length that is substantially the same as an electrically optimum physical length or the an adjustment of the electrically optimum physical length to account for non-electrical considerations,

wherein the wire interconnects a subset of the plurality of function blocks.

**Claim 15 (Currently Amended):** A method to interconnect a plurality of function blocks within a programmable logic device, comprising:

determining a physical length that is electrically optimum for a wire;  
adjusting the determined physical length to account for non-electrical considerations;  
providing the wire having a physical length that is substantially the same as the determined physical length; and  
connecting the plurality of function blocks to the wire,  
wherein a logical length of the wire is a function of an orientation of the wire.

**Claim 16 (Cancelled)**

Claim 17 (Currently Amended): The method of claim 1615 wherein the non-electrical considerations include at least one of the routing efficiency of the wire at the physical length that is electrically optimum and the pattern of connections to the wire.

Claim 20 (Currently Amended): Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a first subset of a plurality of wires having a first logical length and a physical length for transmitting signals between the function blocks; and

a second subset of the plurality of wires having a second logical length and a physical length that is substantially the same as the physical length of the first subset of the plurality of wires for transmitting signals between the function blocks, wherein

the first logical length differs from the second logical length, and

the physical length of the first subset of the plurality of wires is substantially the same as an electrically optimum physical length or the ~~an~~ adjustment of the electrically optimum physical length to account for non-electrical considerations.

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